cosylab
CONTROL SYSTEM LABORATORY

# Control Sheet

Cosylab's newsletter

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## Are companies more expensive than in-house development?

BY: MARK PLESKO (COSYLAB)

I was a researcher working in accelerator labs for some 20 years and I had a very bad opinion about companies, because they were out there to make profits, while we were working for free, or so we thought. Now, I am an entrepreneur for nearly 10 years and I see the other side. The truth is, there is no good or bad side, there are just two different cultures. Maybe the best illustration of the misconception most of the people working in the labs have about companies is the following quote from a friend of mine that works in a famous accelerator laboratory: "Labs pay only salaries, while companies pay salaries plus profit, therefore companies must be more expensive."

Actually, this argument assumes that all people are equally efficient, which turns out to be completely wrong. Our experience is that we are measureable 2-4 times more effective in the work we do, as compared to labs. I can only speak for Cosylab, but I am convinced that the situation is similar for other companies in our field. Now how can this be? Surely the people in labs are smarter than we are? The point is, being smart is only one aspect of effectiveness. Actually, we really try hard to get the smartest people; therefore our recruiting process is much more stringent and meticulous than in labs. But the real challenge in larger projects, which a single person cannot handle alone, is how to make teamwork effective. At Cosylab, we have used our 10 years of experiences in hundreds of projects to optimize our processes and quality assurance to a level that is nearly impossible to match for labs. And why should they? They are researchers, in a way optimized for creativity, while we must be result-oriented. After all, knowing that you won't get paid if the control system doesn't work, does help to overcome the last mile, even when you don't feel like working.

So even if we charge twice our salaries, we are still cheaper than labs. And this is exactly why our offer is so cost-effective and attractive to labs, while we can still make a living. Apart from the fact that we don't have any fancy offices and no perks for the management. So we don't even behave or act like those "evil" profit-oriented companies.

## Cosy-shirts over the globe — photo contests!

Hi, you might remember from the previous Control sheet [1], that we are offering new Cosylab T-Shirts for pictures of you with old Cosylab T-Shirts.

How to play this "game":

Give us feedback [2] by sending us a photo of people wearing Cosylab T-shirts. A photo of you, your collegues, your kids, wife, the prime minister, or anybody else. We will acknowledge the best or funniest photos by publishing them in the newsletter and by sending you another Cosylab T-shirt of your choice.

The first guys with a new Cosylab t-Shirt are Ralph Lange and Mauro Giacchini.

*[1]* Control sheet: *Volume 7*

*[2]* mail to: *controlsheet@cosylab.com*

-----Original Message-----

From: Ralph Lange

Cc: Mauro Giacchini

Subject: Cosylab T-Shirt Photo

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Hello controlsheet!

Of course I have cosylab t-shirt photographs!

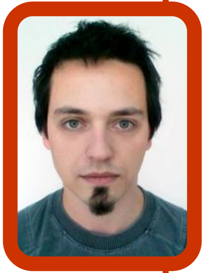
Find attached Mauro Giacchini and me wearing perfectly appropriate shirts for a major dust control job in the kitchen of our temporary home here on Long Island (Mauro was living with us when he visited BNL last fall). Enjoy and best wishes from the beach,

Ralph Lange.

*Proud owners of new Cosylab T-Shirts: Mauro & Ralph*

# CCCP - Cosylab Common Control Platform

BY: MIHA RESCIC, ZIGA KROFLIC (COSYLAB), PETER MEDVESCEK (COBIK*)



Development of a control system is never an easy nor a straightforward task. With the complexity of today's technologies the number of different components or building blocks of the control systems and the complexity overall grow rapidly.

Within this rapidly expanding field it is very difficult to find a common ground and usually much effort is spent on developing highly specific solutions capable of tackling only a limited problem set. Thinking of common grounds in control systems brings to mind a reusable, as generic as possible platform that would represent the core of the system.

But it was not the big accelerator control systems that were the main motivation and the target for CCCP. Not only does CCCP represent a radical shift from custom to generic, it also aims away from common (accelerator) control systems, at the actual products on the market.

This was the motivation behind CCCP: develop a common platform for many different products from the same vendor that would share the control platform but would differ significantly in functionality. Therefore, minimize the efforts needed for core platform development and put emphasis on more specific and complex components, integration, testing and QA.

The platform's most crucial element is the architecture. CCCP keeps logical entities separated as much as possible and thus allows reusability and efficient design.

*1. Custom input / output board*

On the lowest level of CCCP architecture is the customized IO board. The main functions are:

- target hardware development away from the platform core and towards specific implementations,
- provide advanced logic support with FPGA,
- connectivity with existing (or custom) IOs.,
- minimize the complexity of HW and the amount of redundant development efforts.

*2. Device drivers and hardware support*

The layer residing directly above the custom IO board (the lowest layer of core architecture) provides all the logic needed to communicate with hardware:

- OS specific drivers for basic system input / output functionality,
- HW modules as interfaces between the underlying hardware components and higher-level device logic.

*3. Low level device logic*

The low level device logic incorporates all the services and mechanisms needed for the platform to function properly. They lay the foundation for the higher layer logic and provide tools that allow faster development:

- HTTP server for northbound comunication and control,
- priority task scheduler with support of HW modules interrupts,
- lightweight database for data storage, events and logging,
- generic FIFO queues for inter-process data exchange.

*4. High level device logic*

The highest architectural layer is where the magic happens. This layer, also called the "instrument" logic layer, is developed entirely with the scripting language **lua**. This scripting language has these advantages over a programming language:

- complex implementations are done in lower layers thus abstracted away from the developer,
- simpler syntax, robustness and user friendliness of a scripting language make development available to a wider range of developers, e.g. engineers.

The most important aspect of CCCP is the possibility to substitute real hardware components with mock or simulated components. The discrete architectural layering allows a smooth interchangeability between real hardware and software-simulated components. The hardware modules are essentially exposed to higher level device logic so it is simple to make the switch after all interfaces have been defined. The simulated device components are implemented at a higher level (in the high-level instrument logic layer) therefore they override any actual hardware components.

Cosylab Common Control Platform presents a different approach to a rigid field of hardware development. With the modular approach regarding hardware and software architecture, simple input and output interfaces, flexible scripting language core logic and device component simulation capabilities it gives our customers a number of benefits:

- faster time to market with lower development costs,
- better developer utilization and efficiency,
- faster hardware integration, validation and verification,
- maximized flexibility with minimized overdevelopment and complexity.

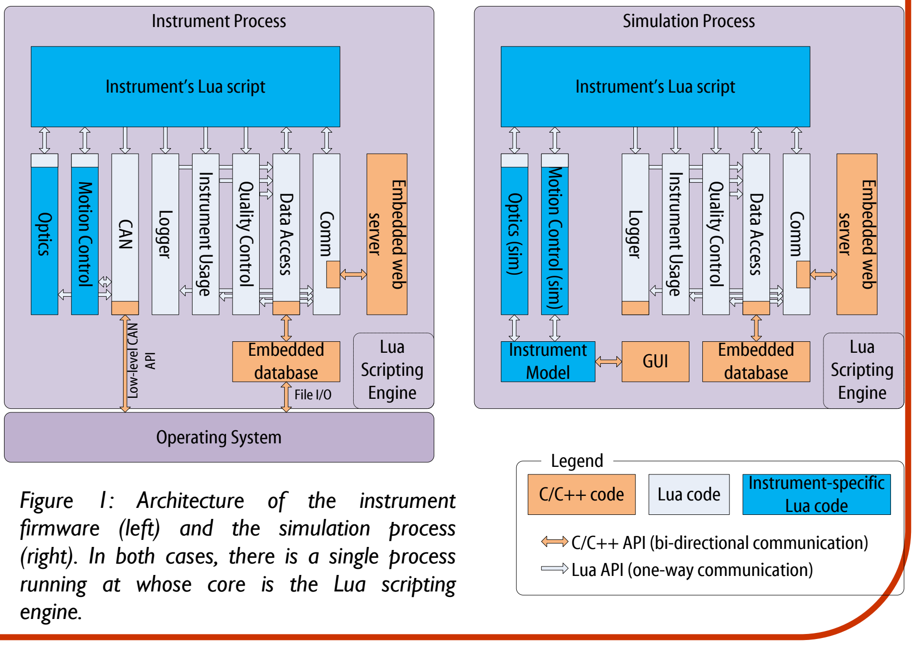


*Figure 1: Architecture of the instrument firmware (left) and the simulation process (right). In both cases, there is a single process running at whose core is the Lua scripting engine.*

* The Centre of Excellence for Biosensors, Instrumentation and Process Control - COBIK, Velika pot 22, SI-5250 Solkan, Slovenia COBIK is an operation financed by the European Union, European Regional Development Fund and Republic of Slovenia, Ministry of Higher Education, Science and Technology."

# CosyBricks FPGA - getting a fresh HW team ready for action

BY: ROK TAVCAR, JOZE DEDIC (COSYLAB), BOJAN ZALAR (COBIK*)

In the past few years, as Cosylab's HW team achieved many great successes, its responsibilities and work opportunities have grown a lot. This also means that the team has to grow – but what do you do with a bunch of HW and FPGA rookies (I can use that word 'cause I was one of them)? In order to bring a fresh HW-team member up to speed with Cosylab's standards regarding coding, implementation and documentation, along with knowledge about basic concepts met regularly in hardware development, the CosyBricks FPGA internal project was born. Its goal was to develop a versatile platform with a low-end FPGA, along with a set of VHDL designs for hardware modules (ADC, DAC, GPIO, etc.) which are commonly used in HW projects. The modular design and a uniform interface between modules reminded us of the famous Danish company's brick toys which we went crazy for when we were kids – hence the project's name. The HW team would gain a set of commonly used building blocks, which could be put together into a working system upon customer demand very quickly.

The effort was organized in the following manner. Each member had to iterate through requirements with the customer (boss), define the architecture of his module and write specifications. He had to stay within budget, adhere to coding standards and deliver a working module accompanied by high quality documentation (document and wiki page). Each module was developed as a final task for the Cosylab FPGA Academy, which every new Cosylab HW team wannabe™ has to go through. The developed platform with its modules was also meant for use in Cosylab's EPICS and LabView Academies.

The CosyBricks base board houses a Spartan 3A FPGA. It has two onboard clocks (10MHz and 16MHz), JTAG connector for programming FPGA and FLASH, 8 connectors (Brick I/F) for connecting modules and an additional 40pin I/O connector. Each module, developed in VHDL, comes with its own I/O board which connects to the base platform via CosyBricks I/F. The developed modules include:

- analog to digital converter – BrickADC,
- digital to analog converter – BrickDAC,
- simple motion controller (single axis control) – BrickSMC,
- general purpose Input/Output – BrickGPIO,
- high-speed Interface – Brick HiSpeedIF.

The base board can be accessed via USB to serial converter (FTDI232), RS232 serial interface and a RJ45 connector for Serializer-Deserializer communication with another board for high speed data transfer (up to 660MHz).

Since the successful finish of the project, new modules have filled our toy box further, e.g. a fiber communication module with clock and data recovery. Through academies EPICS support for BrickADC, BrickDAC and BrickSMC has been developed. The project has achieved its purpose: to quickly bring a team of rookies to production level skills.

CosyBricks FPGA was also a project management exercise for the (fresh) project manager and everybody involved have gained valuable experience in project dynamics from start to finish. Its members are now fully integrated into Cosylab's HW development projects, many of which rely on CosyBricks FPGA as the rapid prototyping platform of choice - we like to think of CosyBricks as programmable particles which greatly accelerate our development processes ;)

All documentation, schematics, VHDL code and EPICS support sources are freely available upon request via email (joze.dedic@cosylab.com). If you are interested in a custom solution based on the CosyBricks FPGA family of modules, feel free to contact us!

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# Ethernet as a real-time network

BY: KLEMEN ZAGAR, KLEMEN VODOPIVEC (COSYLAB), ROK STEFANIC (COBIK*)

Some control applications require a control loop that is **fast**, **distributed** and **hard real-time**. Among them are fast orbit feedback in synchrotron light sources [1], vertical plasma stabilization in tokamaks [2] and adaptive optics in large optical telescopes [3].

By *fast* we mean that the update rate is in the order of several kHz. *Distributed* implies that the sensors, control algorithms and actuators are not all residing on the same computer, but rather on multiple interconnected computers (e.g., due to the size of the system under control, or capabilities of individual computers). *Hard real-time* constraint requires that there is an upper bound on the sensor-to-actuator latency – a necessity for stability of a control loop.

One way to meet the requirements is to develop a custom solution. With somewhat more relaxed requirements, common off-the-shelf (but proprietary) technologies such as reflective memory can be used (e.g., [4]).

Historically, Ethernet was deemed as unsuitable for real-time network applications, particularly due to its inherently non-deterministic *Carrier Sense Multiple Access With Collision Detection* (CSMA/CD) media access protocol. However, in switched full-duplex networks, the probability of collisions is fully eliminated. Instead, non-deterministic queuing delay can occur on switches, but it is possible to use traffic prioritization via the IEEE 802.1p standard to bound it as well.

Ethernet has several advantages. Most importantly, it is a mainstream technology with a large market share and install base. Therefore, the risk of its obsolescence is, at present, small. Also, there is a large number of competing providers of Ethernet services and products in the marketplace. Furthermore, Ethernet is an evolving technology: from 10Mbs 20 years ago, 10Gbps bandwidths are now commonplace, with 40Gbps and 100Gbps standards just ratified.

So, why not use Ethernet as a real-time network? Experiments [5][6] show that the main source of non-determinism is the operating system and its implementation of the network stack. With proper choice and configuration of software, hard real-time constraints can be met! For example, when we have used Xenomai real-time patch for the Linux kernel and RTnet UDP stack implementation [7], we were able to achieve a jitter of end-to-end (sensor-controller-actuator) latency below 10 microseconds even for very large data packets (see Figure 1), which is sufficient for many real-time control applications.

[1] J. Rowland et al.: *Status of the Diamond Fast Orbit Feedback System*, ICALEPCS'07

[2] F. Sartori et al: *The PCU JET Plasma Vertical Stabilization Control System*, 7th Technical Meeting on Control, Data Acquisition and Remote Participation for Fusion Research, Aix-en-Provence, France, 2009

[3] M. Dimmler et al: *E-ELT Primary Mirror Control System*, SPIE Astronomical Telescopes and Instrumentation 2008

[4] K. H. Kim et al: *The Integrated Control System for KSTAR*, ICALEPCS'05

[5] A. Barbalace et al: *Performance Comparison of VxWorks, Linux, RTAI, and Xenomai in a Hard Real-Time Application*, IEEE Transactions on Nuclear Science, 2008

[6] K. Zagar et al: *Evaluation of high-performance network technologies for ITER*, Fusion Engineering and Design, 2010

[7] RTnet: http://www.rtnet.org

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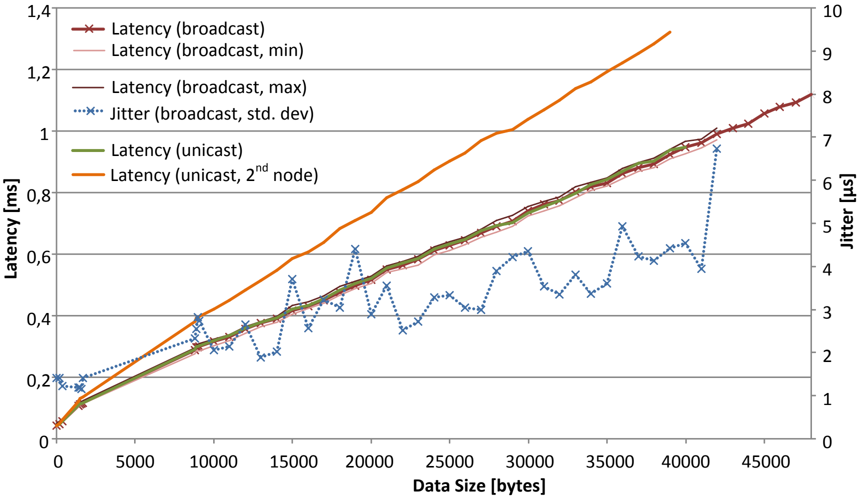

*Figure 1* – latency (left axis) and jitter (right axis) of transmitting a UDP datagram of various sizes from a sensor node, via a control algorithm node, to an actuator node.

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